CLAIMS

What is claimed is:

1. A method for a processor, having a register file comprising a plurality of registers and a broadcast specifier corresponding to the register file, to selectively broadcast via a coprocessor communication bus, write transactions to said register file, the method comprising:
   receiving an operand to be written to said register file;
   selecting one of said plurality of registers in said register file;
   providing to said register file said operand to be written to said register file; and
   selectively providing via said coprocessor communication bus said operand to be written in said register file based on the broadcast specifier.

2. The method of claim 1, wherein the broadcast specifier comprises a set of broadcast indicators, each broadcast indicator within the set of broadcast indicators corresponding to one of the plurality of registers.

3. The method of claim 2, wherein selectively providing via said coprocessor communication bus said operand to be written in said register file is based on the broadcast indicator corresponding to the selected one of said plurality of registers in said register file.

4. The method of claim 1, wherein the broadcast specifier is one of a plurality of broadcast specifiers within the processor, each of the

plurality of broadcast specifiers corresponding to at least one broadcast region of the processor.

5. The method of claim 4, further comprising:

selectively providing, via said coprocessor communication bus, a region indicator corresponding to a current broadcast region of a current write transaction.

6. A method for a first processor, coupled to a second processor via a coprocessor communication bus, to selectively alter an execution mode of said first processor, comprising:

receiving, via said coprocessor communication bus, a region indicator from said second processor, wherein the region indicator indicates a current execution region of the second processor; and

selectively altering the execution mode of said first processor in response to the region indicator.

7. The method of claim 6, wherein altering the execution mode of said first processor comprises altering a functionality of said first processor.

8. A method for a first processor, coupled to a second processor via a coprocessor communication bus, to selectively alter an execution mode of said first processor, comprising:

receiving, via said coprocessor communication bus, a register specifier from said second processor, wherein the register specifier indicates a selected register within a register file of said second processor into which an operand is being written; and

selectively altering the execution mode of said first processor in response to the register specifier.

9. A method for a processor, having a register file comprising a plurality of registers, to selectively broadcast via a coprocessor communication bus, write transactions to said register file, the method comprising:

receiving an operand to be written to said register file;

selecting one of said plurality of registers in said register file;

providing to said register file said operand to be written to said register file; and

selectively providing via said coprocessor communication bus said operand to be written in said register file based on a current execution region of said processor.

10. A processor, comprising:

a plurality of registers;

circuitry for performing a write operation to one of the plurality of registers;

conductors for providing an operand for the write operation to said one of the plurality of registers;

a set of broadcast specifiers;

compare circuitry for comparing the one of the plurality of registers and a selected one of the broadcast specifiers and for providing a broadcast enable signal; and

a port, coupled to the compare circuitry, for communicating with a coprocessor communication bus, said port comprising at least one coprocessor communication bus signal for selectively

providing said operand in response to the broadcast enable signal.

11. The processor of claim 10, wherein each broadcast specifier within the set of broadcast specifiers comprises a set of broadcast indicators.

12. The processor of claim 11, wherein each broadcast indicator corresponds to at least one of the plurality of registers.

13. The processor of claim 10, further comprising:

a program counter unit, for indicating address locations; and

a broadcast region control unit, coupled to the program counter unit, for indicating when the indicated address location from the program counter unit falls within one of a set of broadcast regions.

14. The processor of claim 13, wherein the port further comprises at least one coprocessor communication bus signal indicating a current broadcast region from the set of broadcast regions when the indicated address location falls within one of the set of broadcast regions.

15. The processor of claim 13, wherein the broadcast region control unit comprises a plurality of region storage devices, wherein each broadcast region within the set of broadcast regions has a corresponding region storage device.

16. The processor of claim 15, wherein each region storage device comprises an upper bound storage device and a lower bound storage device to define each broadcast region.

17. The processor of claim 15, wherein each region storage device comprises a base location storage device and a mask storage device to define each broadcast region.

18. A processor, comprising:

a plurality of registers;

circuitry for performing a write operation to one of the plurality of registers;

conductors for providing an operand for the write operation to said one of the plurality of registers;

a program counter unit, for indicating address locations;

an execution region control unit, coupled to the program counter unit, for indicating when the indicated address location from the program counter unit falls within one of a set of execution regions; and

a port, coupled to the compare circuitry, for communicating with a coprocessor communication bus, said port comprising at least one coprocessor communication bus signal indicating a current execution region from the set of execution regions when the indicated address location falls within one of the set of execution regions.

19. The processor of claim 18, wherein said port further comprises:

at least one coprocessor communication bus signal for selectively providing said operand to be written to said one of the plurality of registers during said write operation based on the current execution region.

20. The processor of claim 18, wherein the execution region control unit comprises a plurality of region storage devices, wherein in each execution region within the set of execution regions has a corresponding region storage device for defining the execution region.